Your search matched **14** of **283** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

((scan <near/2> chain) and (pyr >= 1950 and pyr <= Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Automated synthesis of phase shifters for built-in self-test applicati**
Rajski, J.; Tamarapalli, N.; Tyszer, J.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 19 , Issue: 10 , Oct. 2000
Pages:1175 - 1188

[Abstract] [PDF Full-Text (320 KB)] **IEEE JNL**

---

2 **Design of partially parallel scan chain**
Higami, Y.; Kinoshita, K.;
European Design and Test Conference, 1997. ED&TC 97. Proceedings , 17-20 March 1997
Pages:626

[Abstract] [PDF Full-Text (96 KB)] **IEEE CNF**

---

3 **Partially parallel scan chain for test length reduction by using retim technique**
Higami, Y.; Kajihara, S.; Kinoshita, K.;
Test Symposium, 1996., Proceedings of the Fifth Asian , 20-22 Nov. 1996
Pages:94 - 99

[Abstract] [PDF Full-Text (568 KB)] **IEEE CNF**

---

4 **Relay propagation scheme for testing of MCMs on large area substri**
Sasidhar, K.; Chatterjee, A.; Zorian, Y.;
European Design and Test Conference, 1996. ED&TC 96. Proceedings , 11-14 March 1996
Pages:131 - 135

[Abstract] [PDF Full-Text (424 KB)] IEEE CNF

---

5 **A technique for fault diagnosis of defects in scan chains**
Ruifeng Guo; Venkataraman, S.;
Test Conference, 2001. Proceedings. International , 30 Oct.-1 Nov. 2001
Pages:268 - 277

[Abstract] [PDF Full-Text (877 KB)] IEEE CNF

---

6 **Automated synthesis of large phase shifters for built-in self-test**
Rajski, J.; Tamarapalli, N.; Tyszer, J.;
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
Pages:1047 - 1056

[Abstract] [PDF Full-Text (1004 KB)] IEEE CNF

---

7 **Deterministic BIST with multiple scan chains**
Kiefer, G.; Wunderlich, H.-J.;
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
Pages:1057 - 1064

[Abstract] [PDF Full-Text (556 KB)] IEEE CNF

---

8 **Design of phase shifters for BIST applications**
Rajski, J.; Tyszer, J.;
VLSI Test Symposium, 1998. Proceedings. 16th IEEE , 26-30 April 1998
Pages:218 - 224

[Abstract] [PDF Full-Text (212 KB)] IEEE CNF

---

9 **Multi-frequency, multi-phase scan chain**
Kee Sup Kim; Schultz, L.;
Test Conference, 1994. Proceedings., International , 2-6 Oct. 1994
Pages:323 - 330

[Abstract] [PDF Full-Text (516 KB)] IEEE CNF

---

10 **Diagnosis of reconfigurable two-dimensional arrays using a scan approach**
Salinas, J.; Lombardi, F.;
Wafer Scale Integration, 1994. Proceedings., Sixth Annual IEEE International Conference on , 19-21 Jan. 1994
Pages:179 - 187

[Abstract] [PDF Full-Text (360 KB)] IEEE CNF

---

11 **Enhanced reduced pin-count test for full-scan design**
Vranken, G.; Waayers, T.; Fleury, H.; Lelouvier, D.;
Test Conference, 2001. Proceedings. International , 30 Oct.-1 Nov. 2001
Pages:738 - 747

[Abstract] [PDF Full-Text (1369 KB)] IEEE CNF

---

12 **Scan parallel loading in VHDL**
Vo, J.P.;
Verilog HDL Conference and VHDL International Users Forum, 1998. IVC/VIUI Proceedings., 1998 International , 16-19 March 1998
Pages:178 - 187

[Abstract] [PDF Full-Text (32 KB)] **IEEE CNF**

---

13 **Layout-driven chaining of scan flip-flops**
Lin, K.-H.; Chen, C.-S.; Hwang, T.T.;
Computers and Digital Techniques, IEE Proceedings- , Volume: 143 , Issue: 6 , Nov. 1996
Pages:421 - 425

[Abstract] [PDF Full-Text (524 KB)] **IEE JNL**

---

14 **Design of compactors for signature-analyzers in built-in self-test**
Wohl, P.; Waicukauski, J.A.; Williams, T.W.;
Test Conference, 2001. Proceedings. International , 30 Oct.-1 Nov. 2001
Pages:54 - 63

[Abstract] [PDF Full-Text (979 KB)] **IEEE CNF**
